

# Ordered Arrays of $\langle 100 \rangle$ -Oriented Silicon Nanorods by CMOS-Compatible Block Copolymer Lithography

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## ABSTRACT

Dense, ordered arrays of  $\langle 100 \rangle$ -oriented Si nanorods with uniform aspect ratios up to 5:1 and a uniform diameter of 15 nm were fabricated by block copolymer lithography based on the inverse of the traditional cylindrical hole strategy and reactive ion etching. The reported approach combines control over diameter, orientation, and position of the nanorods and compatibility with complementary metal oxide semiconductor (CMOS) technology because no nonvolatile metals generating deep levels in silicon, such as gold or iron, are involved. The Si nanorod arrays exhibit the same degree of order as the block copolymer templates.

One-dimensional (1D) semiconductor nanostructures exhibit electronic, optical, chemical, mechanical, and thermal properties that depend on their diameter and on their growth direction.<sup>1</sup> Silicon (Si) nanowires are of particular interest, as state-of-the-art semiconductor technology is still based on this material. Two strategies for the fabrication of assemblies of Si nanowires have been investigated: vapor–liquid–solid (VLS) growth, and combinations of block copolymer (BCP) lithography and reactive ion etching (RIE). These approaches involve the use of etch resists or catalysts consisting of metals such as gold (Au) or iron (Fe), which are incompatible with complementary metal oxide semiconductor (CMOS) technology. Gold and iron as well as cobalt and nickel can contaminate silicon,<sup>2</sup> thus generating deep levels in the band gap of this semiconductor.<sup>3</sup> The presence of deep levels deteriorates the electronic properties of Si because they act as efficient centers for the recombination of electrons and holes. Therefore, the development of a fabrication process that circumvents the use of metals generating deep levels is a prerequisite for the technical

exploitation of Si nanowire arrays. We report a CMOS-compatible procedure for the formation of dense, ordered Si nanorod arrays with a lattice constant of 36 nm based on BCP lithography and plasma etching that meets this requirement. Diameter, orientation, and position of the nanorods with aspect ratios (length/diameter) of 5:1 and diameters of 15 nm can easily be controlled. CMOS devices are commonly fabricated on (100) Si wafers to achieve optimal electronic performance of the gate oxides. To realize a configuration that enables the combination of standard CMOS devices with components based on vertical Si nanorods, we generated Si nanorod arrays with the  $\langle 100 \rangle$  direction perpendicular to the surface of an (100) Si wafer.

Vapor–liquid–solid (VLS) growth, which is initiated and catalyzed by gold<sup>4–7</sup> or aluminum<sup>8</sup> nanoparticles, commonly yields  $\langle 111 \rangle$  or  $\langle 110 \rangle$  oriented nanowires. Gold colloids,<sup>9,10</sup> thin Au<sup>11</sup> and Al<sup>8</sup> films, nanosphere lithography,<sup>12</sup> gold-implanted Si substrates,<sup>13</sup> and galvanic displacement processes<sup>14</sup> were employed to generate and to position metal nanoclusters, whose size and location determine the diameter and the position of the Si nanowires. However, metal clusters incommensurate with the underlying substrate in nonepitaxial systems exhibit high diffusivity,<sup>15,16</sup> particularly at the elevated temperatures<sup>17</sup> required for the growth of Si nanowires. Therefore, VLS-based methods do not allow

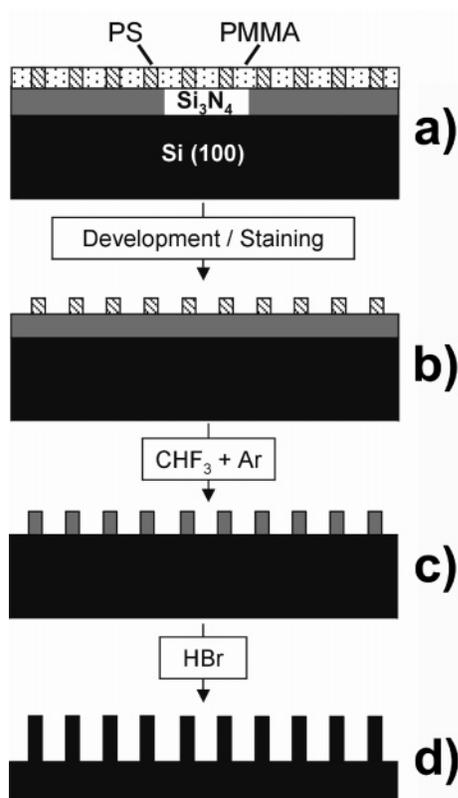
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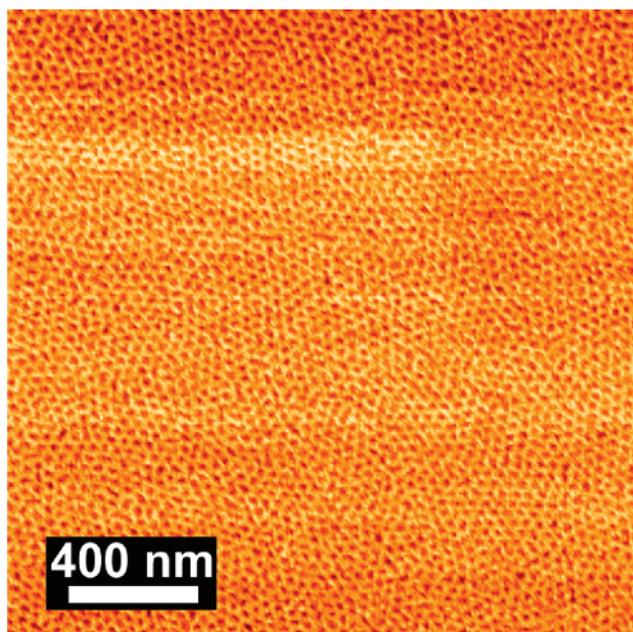
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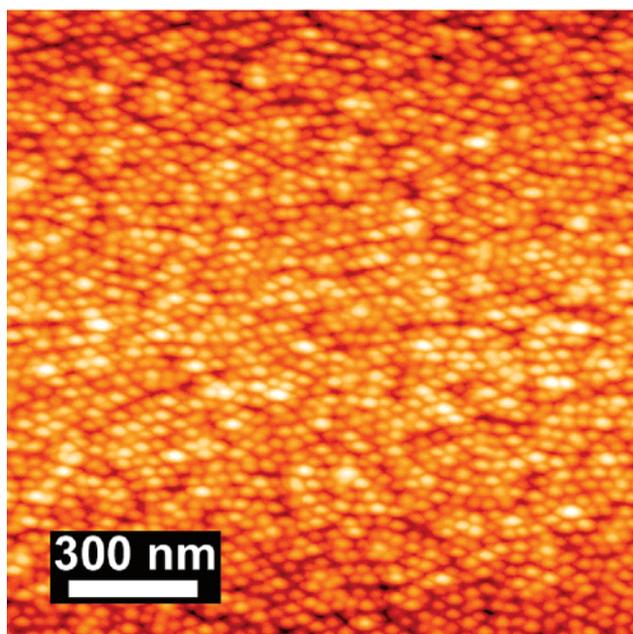


**Figure 1.** Schematic diagram of the fabrication procedure for Si nanorod arrays by BCP lithography. (a) A 35 nm thick PS-*b*-PMMA film containing PS cylinders normal to the film plane forms on a Si<sub>3</sub>N<sub>4</sub>-coated Si wafer. (b) Selective removal of the PMMA yields an ordered array of PS nanodots. (c) The pattern thus generated is transferred into the Si<sub>3</sub>N<sub>4</sub> layer by RIE with a CHF<sub>3</sub>/Ar mixture. (d) The ordered array of Si<sub>3</sub>N<sub>4</sub> nanodots acts as an etch mask for the formation of Si nanowires by RIE with HBr.

assembling dense, ordered arrays of  $\langle 100 \rangle$  oriented Si nanowires with periods in the sub-50 nm range. Block copolymer (BCP) lithography combined with plasma etching is an alternative approach that potentially overcomes these drawbacks. BCPs self-assemble into ordered arrays of nanoscopic domains, whose nature depends on the relative composition of the BCP.<sup>18–21</sup> The selective removal of one component yields etch masks for the patterning of underlying substrates<sup>22–30</sup> by plasma etching.<sup>31</sup> Commonly, these masks contain hexagonal arrays of holes within a continuous matrix. A tedious mask reversal process that started with the fabrication of a continuous porous film involving several deposition and etching steps, each of which may give rise to defects and artifacts, yielded Si nanopillars.<sup>29</sup> However, the direct generation of pillar arrays by BCP templates consisting of dot arrays is much more attractive because the number of process steps and the related costs could be reduced, whereas the throughput could be improved. Park et al. proposed BCP templates containing hexagonal arrays of spherical polybutadiene (PB) domains stained with osmium embedded into a polystyrene (PS) matrix as templates for the production of nanodot arrays.<sup>22</sup> However, wetting layers consisting of PB at the BCP/air and BCP/substrate interfaces are a severe drawback for the pattern transfer by dry etching. The generation of nanorod arrays by plasma



(a)



(b)

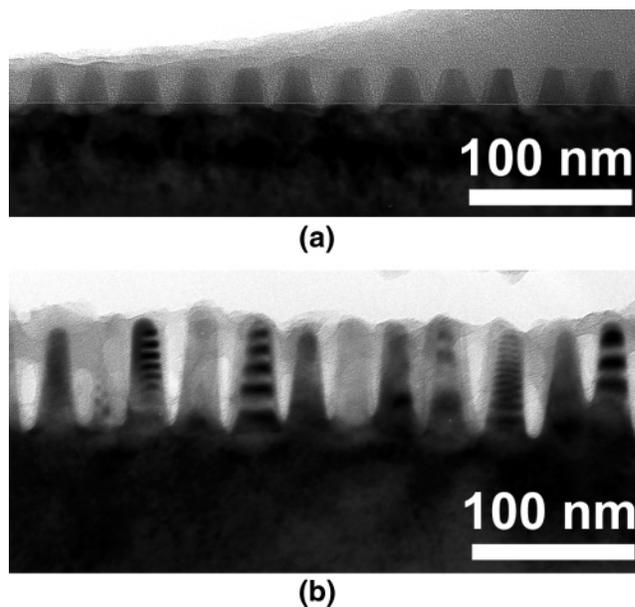
**Figure 2.** Atomic force micrographs of the BCP template prior to and after the removal of PMMA. (a) Phase image of a 35 nm thick PS-*b*-PMMA film after annealing for 40 h at a temperature of 165 °C. The PS domains appear dark, the PMMA matrix appears bright. (b) Topography image of an array of PS nanodots after the removal of the PMMA.

etching requires robust masks with high etch contrast. Configurations based on spherical particles without adhesive contact to the substrate do not meet this requirement. Organometallic polymers containing spherical ferrocenyldimethylsilane (PFS) domains within a PS matrix may overcome this drawback and allow transferring the pattern defined by the PFS domains into underlying substrates.<sup>25</sup> However, the nonvolatile Fe-containing contaminations pose a serious problem for CMOS technology. This is also the

case if block copolymer micelle nanolithography<sup>32,33</sup> is employed to position arrays of spherical metal nanoparticles.

Etch masks consisting of cylinders connected to the underlying substrate show better etch contrast and better robustness. Therefore, such inverse etch masks allow the use of resists based on nanoparticles containing significant amounts of Fe, Au, or other nonvolatile metals, generating deep levels to be circumvented. We fabricated arrays of cylindrical PS domains instead of the commonly used porous continuous films from a polystyrene-*block*-poly(methyl methacrylate) (PS-*b*-PMMA) template with a PS volume fraction of 30% for the CMOS-compatible generation of Si nanorod arrays. A 35 nm thick Si<sub>3</sub>N<sub>4</sub> layer was deposited onto (100)-oriented silicon wafers by low-pressure chemical vapor deposition. Hydroxyl-terminated random copolymers of styrene and methylmethacrylate were grafted onto the Si<sub>3</sub>N<sub>4</sub> surface as previously described<sup>34</sup> to balance the interfacial interactions of PS and PMMA. A 1 wt % solution of PS-*b*-PMMA ( $M_w = 75.6$  kg/mol,  $M_n = 70.7$  kg/mol,  $M_w/M_n = 1.07$ ; Polymer Source Inc.) in propylene glycol monomethyl ether acetate (Aldrich) was spin-coated onto the wafers thus treated to produce a 35 nm thick BCP film, as determined by ellipsometry (Figure 1a).<sup>35</sup> The samples were annealed for 40 h at a temperature of 165 °C under nitrogen. As a result, PS cylinders oriented normal to the substrate formed within the PMMA matrix. The latter was removed by exposure to UV light for 5 min, followed by rinsing with acetic acid. The PS was stained with ruthenium tetroxide (RuO<sub>4</sub>)<sup>36</sup> to enhance the contrast in the subsequent dry etching steps. To this end, we exposed the samples to RuO<sub>4</sub> vapor produced by dissolving 0.2 g ruthenium chloride hydrate (RuCl<sub>3</sub>·3H<sub>2</sub>O, Aldrich) in 10 mL 10 wt % aqueous sodium hypochlorite solution (Aldrich) for 15 min. The staining procedure yields arrays of PS nanodots containing Ru atoms, which exhibit improved chemical and thermal stability (Figure 1b). In contrast to Au and Fe, Ru shows a pronounced tendency toward the formation of volatile compounds<sup>37</sup> and can therefore easily be removed. Theoretical studies revealed that Ru does not generate deep levels in crystalline silicon.<sup>3</sup> This is in line with results indicating an even improved performance of Si/metal oxide solar cells when Ru is incorporated into the oxide layer.<sup>38</sup> The pattern transfer into the underlying Si<sub>3</sub>N<sub>4</sub> was achieved by reactive ion etching (RIE) with a mixture of 10 vol % CHF<sub>3</sub> and 90 vol % Ar for 50 s using an inductively coupled plasma (ICP) reactor (Oxford PlasmaLab System 100) equipped with 2.1 MHz ICP380 and 13.56 MHz radio frequency sources. Si<sub>3</sub>N<sub>4</sub> dots formed at the position of the PS dots, whereas the underlying Si substrate in between was uncovered (Figure 1c). Finally, the exposed Si was etched with HBr for 60 s, forming Si nanorods at the positions of the Si<sub>3</sub>N<sub>4</sub> dots that were removed in the course of this RIE step (Figure 1d).

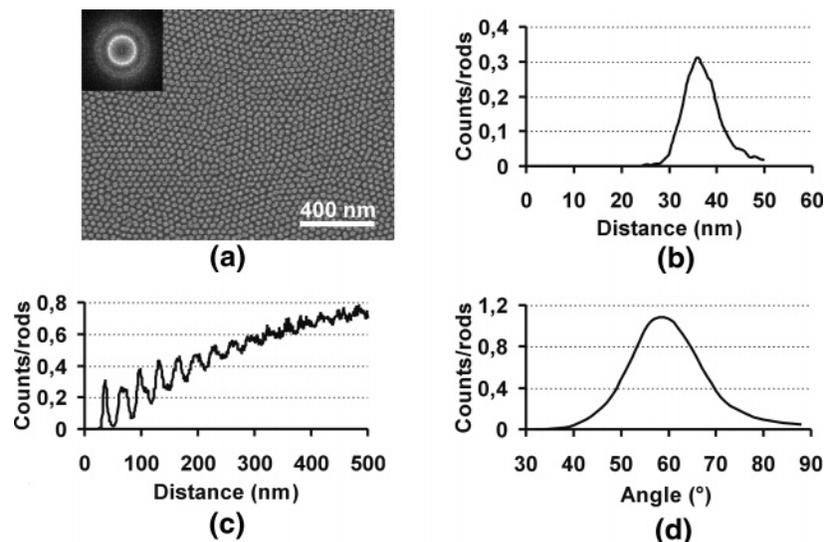
We investigated the BCP films prior to and after the removal of the PMMA by atomic force microscopy (AFM), using a Digital Instruments Inc. 5000-1 AFM equipped with silicon cantilevers (NSC15, MikroMasch, resonant frequency 325 kHz). Figure 2a shows an AFM phase image of a BCP



**Figure 3.** Transmission electron micrographs of cross-sectional specimens (a) of Si<sub>3</sub>N<sub>4</sub> nanodots connected to the underlying Si wafer after the first RIE step with CHF<sub>3</sub>/Ar and (b) of Si nanorods connected to the underlying Si wafer after the second RIE step with HBr. Note that the distinct interface between the Si<sub>3</sub>N<sub>4</sub> layer and the Si substrate seen in (a) vanishes after RIE with HBr, indicating the complete removal of the Si<sub>3</sub>N<sub>4</sub>.

film prior to the removal of the PMMA. The dark PS cylinders with a diameter of 18 nm are surrounded by a bright PMMA matrix. The period of the hexagonal microphase structure amounts to 36 nm. The topography image of a developed sample (Figure 2b) shows the liberated PS cylinders in bright contrast. It is obvious that the removal of the PMMA did not destroy the arrangement of the PS cylinders. After each RIE step, cross-sectional specimens of the samples thus obtained were investigated by transmission electron microscopy (TEM) using JEM 1010 and Phillips CM20T transmission electron microscopes operated at accelerating voltages of 100 and 200 kV, respectively. Cross-sectional specimens were prepared by slicing ~400 μm sections from samples embedded in epoxy resin with a diamond wire. The sections were ground and polished to a thickness of ~80 μm, dimple-ground, and further polished to a thickness less than 15 μm. The samples were then thinned to electron transparency by ion etching from both sides with Ar ions (PIPS, Gatan).

The RIE step with CHF<sub>3</sub>/Ar resulted in the formation of Si<sub>3</sub>N<sub>4</sub> dots with a height of 25 nm and a diameter of 18 nm at the top on the Si substrate (Figure 3a). The period of the array was 36 nm, corresponding to that of the BCP template. Note the clear and distinct interface between the Si and the Si<sub>3</sub>N<sub>4</sub> that is typical of Si<sub>3</sub>N<sub>4</sub> layers deposited on Si by low-pressure CVD.<sup>39</sup> The subsequent RIE step with HBr yielded an array of Si nanorods connected to the Si substrate with diameters of about 15 nm and an aspect ratio of about 5:1. While in this work a proof of concept is demonstrated, higher aspect ratios of the Si nanorods may be realized by optimizing the HBr-based etch protocols or by testing other etch gases. The complete removal of the Si<sub>3</sub>N<sub>4</sub> caps is



**Figure 4.** Scanning electron micrograph and real space image analysis of an array of Si nanorods. (a) SEM image with corresponding Fourier transform (inset). (b) Nearest-neighbor peak of the pair distribution function. (c) Pair distribution function encompassing a length of 500 nm, evidencing that a correlation between the positions of the nanorods exists for distances as large as 500 nm. (d) Angular distribution function, representing the distribution of the angles between three nearest neighbors.

obvious from the disappearance of the Si/Si<sub>3</sub>N<sub>4</sub> interface. The array of the Si nanorods still exhibited a period of 36 nm, as initially imposed by the BCP template (Figure 3b).

The lateral order of the Si nanorod arrays was analyzed by real space image analysis. The scanning electron microscopy image<sup>40</sup> in Figure 4a shows a large field view of an ensemble of Si nanorods. The Fourier transform of a quadratic section of this image with an edge length of 1200 nm shows ring patterns, as expected for nanorod assemblies exhibiting a polycrystalline degree of order. The nearest-neighbor peak in the pair distribution function (PDF) of Figure 4a centers at 36 nm and has a half width at half-maximum of 3.6 nm (Figure 4b). The PDF reveals that a correlation in the Si nanorod array exists up to distances of 500 nm (Figure 4c). The angular distribution function (ADF) seen in Figure 4d represents the distribution of the angles between three nearest neighbors. For an ideal hexagonal lattice, a sharp peak at 60° is to be expected. The ADF of Figure 4a shows a peak centering at 60° with a half width at half-maximum of 7.3°. Therefore, the array of the Si nanorods is a perfect replica of the BCP template, the order of which can be optimized by solvent annealing<sup>41</sup> or the addition of salt.<sup>42</sup>

We have reported an approach to the fabrication of dense, ordered arrays of Si nanorods uniform in orientation and diameter that combines the advantages of BCP lithography and compatibility with CMOS technology. The indispensable dry etching step imposes limitations on the range of realizable aspect ratios. However, BCP lithography enables the rational design of highly ordered Si nanowire arrays with potential long-range order and sharp distribution of the diameters of the nanowires. Future work will aim at the preparation of arrays of complex nanowires containing heterostructures. For example, the use of planar Si/SiGe heterostructures as substrates should yield Si/SiGe nanowires with sharp Si/SiGe interfaces, while such sharp interfaces cannot be realized by

vapor–liquid–solid growth because of the high solubility of Si and Ge in eutectic Au/Si/Ge mixtures.<sup>43,44</sup>

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